REMARKS

In the Office Action, the Examiner rejected Claims 1-16, which are all of the pending claims, under 35 U.S.C. §102 as being fully anticipated by U.S. Patent 5,666,078 (Lamphier, et al.). The Examiner also objected to the drawings.

Independent Claims 1 and 9 are being amended to better define the subject matters of these claims. Claim 3, which is dependent from Claim 1, is being amended to keep the language of Claim 3 consistent with the language of Claim 1; and Claims 10-16 are being amended to keep the language of these claims consistent with the language of Claim 9, from which Claims 10-16 depend.

Applicants are also amending Figure 1 to address the Examiner's objections to the drawings. More specifically, in the Office Action, the Examiner objected to the drawings as not showing the features, described in Claims 1 and 9, that the I/O cell includes a set of resistance devices, and the reference cell includes a copy of that set of resistance devices. Figure 1 is being amended to show schematically a set of resistance devices in I/O cell 12 and a copy of these resistance devices in reference dell 14. Reference numbers are being provided for these resistance devices, and the specification is also being amended to include these reference numbers.

In view of these changes to the drawings, the Examiner is asked to reconsider and to withdraw the objection to the drawings.

With respect to the rejection of the claims over the prior art, an important feature of the present invention, which is considered to be patentable over the prior art, is that this invention provides a method of programmable impedance control that incorporates an ASIC (application specific integrated circuit). Moreover, the control logic portion of the programmable impedance output driver architecture may be designed using standard ASIC library elements, which facilitates the migration of the design to other technologies.

More specifically, this invention relates to an I/O cell having a programmable active input bias. In the invention, a reference cell is used to determine the extent to which a driver impedance of the I/O cell should be adjusted to keep that impedance within a given range of a certain value. The reference cell includes a series of resistance devices that are activated, by a digital controller, to determine a digital signal that is transmitted to the driver to change the impedance of the driver. The I/O cell, the reference cell, and the controller for the reference cell are all part of the same ASIC.

Lamphier, et al. which was cited by Applicants in an Information Disclosure Statement file with this application, does not show or teach this ASIC architecture. In particular, in Lamphier, et al, an off-chip driver 60 is used to determine the desired impedance for the output driver circuit.

The ASIC architecture of the present invention is of utility for a number of reasons. The logical design of the controller is relatively compact and simple, and this leads to the controller's technology-independent nature. Because of this, the controller can be synthesized using primitive and basic logic blocks commonly found in most technology cell libraries. At the same time, the design can be used with many, if not practically any, technology offering

without requiring and redesign of the control circuitry. This dramatically decreases the design time of the programmable impedance I/O scheme.

Independent Claims 1 and 9 clearly describe the above-discussed feature of the invention. Specifically, Claim 1, which is directed to a method of impedance control, positively sets forth the step of providing an application specific integrated circuit including an I/O cell, a reference cell, and a digital controller, and the claim goes on to describe how the reference cell and the digital controller are used to adjust the impedance of the I/O cell.

Similarly, Claim 9 is being amended so that the claim is now positively directed to "An application specific integrated circuit," including an I/O cell and a control circuit for controlling the impedance of the I/O cell. The claim further describes the elements of the control circuit, including a set of resistance devices, a comparator, and a digital generator, and describes how these elements cooperate to adjust the input/output impedance of the I/O cell.

The other reference of record have been reviewed, and it is believed that these other references, whether they are considered individually or in combination, are no more pertinent than Lamphier, et al. In particular, none of these references disclose the way in which the present invention achieves an active-compensation of a programmable impedance I/O in an ASIC architecture.

Because of the above-discussed differences between Claims 1 and 9 and the prior art, and because of the advantages associated with those differences, Claims 1 and 9 patentably distinguish over the prior art and are allowable. Claims 2-8 are dependent from Claim 1 and are allowable therewith. Likewise, Claims 10-16 are dependent from, and are allowable with,

Claim 9. The Examiner is, accordingly, respectfully requested to reconsider and to withdraw the rejection of Claims 1-16 under 35 U.S.C. §102 and to allow these claims.

For the reasons set forth above, the Examiner is asked to reconsider and to withdraw the objection to the drawings and the rejection of Claims 1-16 under 35 U.S.C. §102, and to allow these claims. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

John S. Sensny

John S. Sensny
Registration No. 28,757
Attorney for Applicants

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343

JSS:jy
Enclosure: Proposed Drawing Change to Figure 2